(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 January 2005 (06.01.2005)

PCT

(10) International Publication Number
WO 2005/002019 A1

(51) International Patent Classification[7]: H02H 9/04

(21) International Application Number:
PCT/IB2004/050973

(22) International Filing Date: 23 June 2004 (23.06.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
03101950.8 30 June 2003 (30.06.2003) EP

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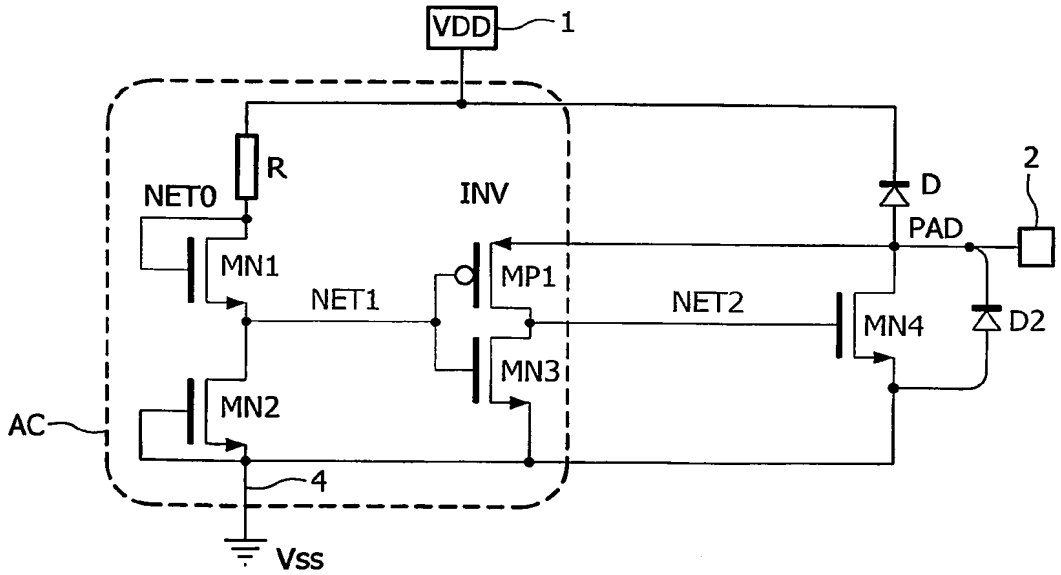
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**
— *with international search report*

*[Continued on next page]*

(54) Title: PROTECTION CIRCUIT FOR AN INTEGRATED CIRCUIT DEVICE




(57) Abstract: The integrated protection circuit according to the invention for ESD protecting an circuit device having at least one pad, e.g. a I/O pad, comprises a first transistor (MP1) whose control outputs are connected between the pad (2, 3) and the control input of a clamp transistor (MN4). The control outputs of the clamp transistor (MN4) are connected between the pad (2, 3) and a reference terminal (4). The protection circuit further comprises a second transistor (MN3) whose control outputs are connected between the control output of the first transistor (.MP 1) and the reference terminal (4). Finally the protection circuit also comprises time-delay elements (R, MN 1) connected between a supply voltage terminal (1) and the control inputs of the first transistor (MP I) and the second transistor (MN3).

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